Lecture 10

Digital-to-Analogue Conversion

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Lecture Objectives

- Understand pulse-width modulated (PWM) DAC
- Understand how a weighted-resister DAC can be used to convert numbers with binary or non-binary bit weightings
- Understand the meaning of the terms used to **specify DAC accuracy**
- Understand resistor string based DAC architecture
- Understand how an R-2R ladder can be used to convert both unsigned and signed binary numbers
- Understand multiplying DAC

References:

• "Data Converter Architectures" in Data Conversion Handbook by Analog Devices

Analogue Pulse-width Modulated (PWM)



Digital Pulse-width Modulated (PWM) as DAC

- Sawtooth value generated by a wrap-around counter
- Load pulse latches data_in and stores it in register
- When input value is reached by counter, comparator output changes state (H to L)
- Lowpass filter provides analogue output voltage proportional to the duty cycle of PWM signal



PWM DAC in SystemVerilog



Simple DAC

• A DAC converts a binary number into a voltage proportional to its value:



- Hence V_{OUT} is a weighted sum of V₃, ..., V₀ with weights proportional to the conductances G₃, ..., G₀.
 - If X3:0 is a binary number we want conductances in the ratio 8:4:2:1.
 - Very fast: gate slew rate > 3 V/ns.
 - We can scale the resistors to give any output impedance we want.
- You do not have to use a binary weighting
 - By using other conductance ratios we can choose arbitrary output voltages for up to five of the sixteen possible values of X3:0. May need additional resistors from VOUT to the power supplies.

Improved DAC with Output Op-Amp



- Adding an op-amp:
 - The voltage at the junction of all the resistors (the virtue earth node) is now held constant by the feedback
 - Hence current drawn from V_3 is independent of the other voltages $V_2, ..., V_0$
 - Hence any gate non-linearity has no effect \Rightarrow more accurate
 - Lower output impedance
 - Much slower: op-amp slew rate \approx 1 V/µs
- Hard to make accurate resistors covering a wide range of values in an integrated circuit
 - Weighted-resistor DAC is no good for converters with many bits

Further Improvement with reference voltage source



DAC Specification Jargon



- Resolution
 - 1 LSB = ΔV when $X \rightarrow X+1$
 - = Full-scale range \div (2^N-1)
- Accuracy
 - Worst deviation from nominal line
- Linearity
 - Worst deviation from line joining end points

- Worst error in ΔV when $X \rightarrow X+1$
- measures smoothness
- Monotonic
 - At least ΔV always has the correct sign

• Settling time

- Time taken to reach the final value to within some tolerance, e.g. $\pm \frac{1}{2}$ LSB

Thermometer DAC using Resistor String



- ✓ Simple
- Inherently monotonic
- Needs only IDENTICAL resistors, good differential linearity
- Only two switches operate during a transition, low output glitch and fast settling
- Low power
- Widely use with modern technology with small feature sizes
- X Large number of resistors
- X Useful for low to medium resolution DAC
- X Large resistance resulting in higher noise

Resistor String DAC with Op-Amp output



DAC using R-2R Ladder

We want to generate currents I_0 , $2I_0$, $4I_0$, ...

Two 2R resistors in parallel means that the 2I₀
Current will solid equally and equivalent resistance R



- The Thévenin resistances of the two branches at V_1 both equal 2R so the current into this node will split evenly
 - We already know that the current into node V_0 is $2I_0$, so it follows that $I_1=2I_0$
- We can repeat this process indefinitely and, using only two resistor values, can generate a whole series of currents where $I_n=2^nI_0$
 - From the voltage drop across the horizontal resistors, we see that $V_n = 2RI_n = 2^{n+1}RI_0$
 - For an *N*-bit ladder the input voltage is therefore $U = 2^{N} D U = 2^{-N} U$

$$V_{in} = 2^{N} R I_0 \Longrightarrow I_0 = 2^{-N} V_{in} / R$$



2R

R

2R

V_o

= 2I_o

Current-Switched DAC

- Total current into summing junction is $X3:0 \times I_0$
 - Hence $V_{out} = X3:0 \times V_{in}/16R \times -R_f$
 - We switch currents rather than voltages so that all nodes in the circuit remain at a constant voltage

 \Rightarrow no need to charge/discharge node capacitances

 \Rightarrow faster



- Each 2-way switch needs four transistors
- As required by R/2R ladder, all the switch output terminals are at 0 V.
 - ladder outputs are always connected either to ground or to a virtual earth



Programmable Attenuator (Amplifier)

 The output of the DAC is proportional to the *product* of an analog voltage (V_{in}) and a digital number (X3:0)

$$V_{out} = X3:0 \times V_{in} / 16R \times -R_f$$

- It is called a *multiplying* DAC
- Can be used as a digital attenuator:



• Here the digital number X7:0 controls the gain of the circuit

The MCP4921 DAC (used in Lab)



Serial Peripheral Interface for DAC (SPI)



Interfacing the FPGA to the DAC



Symbol	Description
V _{DD}	Supply Voltage Input (2.7V to 5.5V)
CS	Chip Select Input
SCK	Serial Clock Input
SDI	Serial Data Input
LDAC	DAC Output Synchronization Input. This pin is used to transfer the input register (DAC settings) to the output register (V_{OUT})
V _{REF}	Voltage Reference Input
V _{SS}	Ground reference point for all circuitry on the device
V _{OUT}	DAC Analog Output



Lab 5 – DAC conversion – Prototype Shield



5V sockets to power analogue board

Insert the prototype shield onto the DE10 sockets

Leave one socket free to connect later

> Add 3 or 4 header pin for GND clips of scope probes

Lab 5 Task 1 PWM as a DAC converter



Lab 5 Task 2 Using the MCP4921 chip

